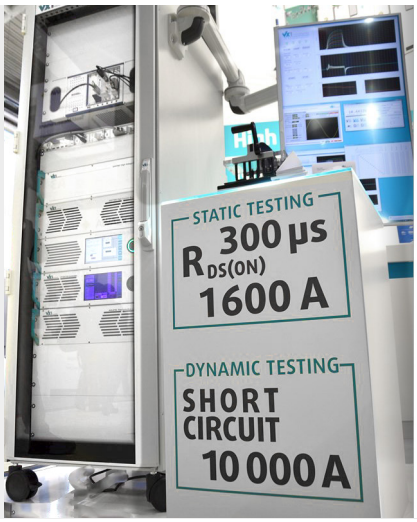
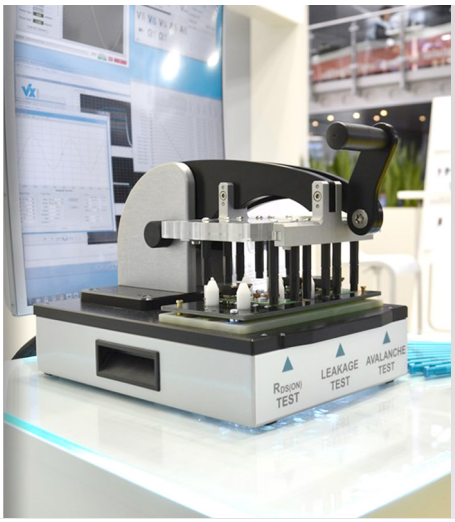
WHITEPAPER

VXI Instruments
the test solutions provider

Cost-reduction and simplification:

1 000 A high current $R_{DS(on)}$ static parameter DC testing vs. pulse testing @ 300 µs





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The need for high-power semiconductors like diodes, MOSFETs, or IGBTs is increasing rapidly. All areas of renewable energy, e-mobility, or industrial electronic drives have a strongly growing need for more powerful components.

Testing these components is a big challenge for test engineers, since currents and voltages have been rising rapidly in the last few years and will continue as such going forward. To cut excess costs in mass volume production, these tests have to be done at different steps in the process, from front-end wafer level, bare-die, to back-end, where the discrete component and final product is tested. On one hand, this is mandatory to ensure consistently high quality and reliability of the devices. On the other hand, it is also important to detect failing parts as soon as possible – avoiding continuous processing of failed parts, and therefore lower production costs. The best cost-saving results can be achieved if you are able to completely cover test specification in every process step. For the most part, this isn't easy. I'll explain why – further along in this article – and provide an example that shows how you can work around problems by calculating for testing the $R_{DS(on)}$ static on-resistance parameter of a MOSFET. Most of that can be adapted to the measurement of V_f forward voltage of a diode or $V_{CE,sat}$ saturation voltage of an IGBT.

$R_{DS(on)}$ static on-resistance parameter of a MOSFET

MOSFETs with $R_{DS(on)}$ drain-source resistance of less than 1m Ohm are already available on the market. Maximum voltages and currents, which can be switched by modern IGBTs like B2/4/6-modules or MOSFETs (see Figure 1), are increasing. According to typical test specifications for $R_{DS(on)}$, the components have to be tested at the maximum ratings, so test currents of 1 000 A or more are required nowadays.

Figure 1:
SOT-227 MOSFET

In this article, we will discuss the advantages and disadvantages of measuring $R_{DS(on)}$ with direct current (DC)-based instruments, and current pulse sources in comparison. DC voltage and DC current sources have slow rise times that settle to a stable current level and need test times from 10 ms or more. Thus, such tests are often performed within 100 ms. Since 100 ms is far away from any time constant of thermal elements in a typical test system setup (e. g. heating of contact pin/needle), we call that kind of testing "DC testing". In comparison, we will show how fast current pulse sources can help to achieve test requirements.

Direct current and the system components

The decision of which method of testing you choose for your test case has a dominant influence on all test system equipment. In one method it has to be DC-capable, and just pulse-capable with the other method. Simplified, a typical test setup for measuring the $R_{DS(on)}$ resistance consists of four different functional units, you should have an eye on:

- Current source
- Cabling
- High-current matrix/multiplexer
- DUT (fixture/needle adapter/wafer prober)

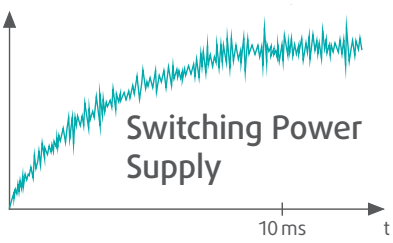

Figure 2: Output signal with ripple.

The used current source itself is very different in design, depending on whether one is performing DC or pulsed testing. High-current DC sources are designed to supply energy continuously, and therefore also have a correlating cooling capability which both result in a larger form factor. Since they are based on switching power supplies, these provide output currents, which do have a certain ripple (see figure 2). It is important to take care of when performing measurements.

Beside the current source, it is the cabling, multiplexer, and the DUT adapter which will all generate – although they are stressed – ohmic and thermal losses when performing high-current tests (see figure 3).

Performing these tests with DC currents significantly increases the required effort for these system components. They have to be capable of handling 1 000 A DC or more, and therefore the thermal power losses generated have to be cooled constantly. This results in devices like DC capable power sources, heavy and very low resistance cabling, big high current switching relays, and the need for many contacting needles. Every component has to be able to handle the system DC currents, so in consequence they are bigger, need a lot of rack and floor space, and are more cost-intensive for operating costs for all the years the DUT should be produced and tested.

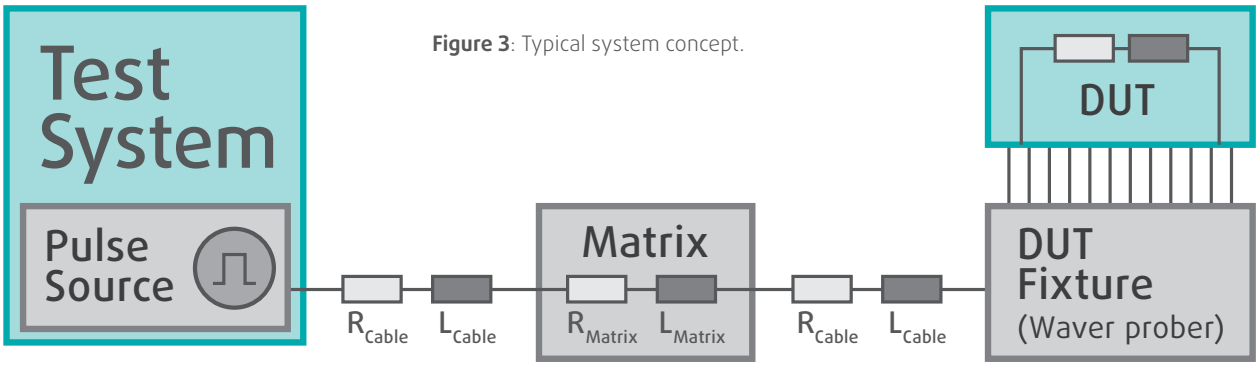

Figure 3: Typical system concept.

High current pulse source

The second way is smarter. By using very fast high current pulse sources, most components of a test system can be run more easily. Testing a device with 1 000 A with a pulse of e. g. 300 µs greatly changes the requirement for the overall performance of system components like matrix or cabling. To realize such a "smart" test system, one challenge that has to be overcome is the reduction of parasitic inductances. By using a pulse source and therefore the possibility to use more smart system components like a smaller matrix, it is possible to reduce the system inductance. Designing low-inductive system components – like a low inductive matrix – needs a lot of know-how but is feasible. In particular, by optimizing the system cabling, there is another great opportunity to reduce parasitic inductances. In addition, the proper selection of connectors, their type, and the amount of contact needles are significant for the system.

As a rough estimate, one can say that initial system hardware cost of DC-capable test system and smart pulse test system may differ not very much. The big advantages of smart test systems are a much smaller space requirement and the ability to achieve a much higher system throughput due to the high test speed, which will additionally reduce cost for testing.

Ohmic resistance and parasitic inductance...

Since the size of these system components are mainly defined by their thermal capability, the Ohm's Law is the major problem to fight. Thermal losses rise exponentially with rising currents:
P = R * I * I (Ohm's Law)

This means: raising the test current by a factor of 2 will raise ohmic power losses in relays, cable, and needles by a factor of 4. Raising the test current by a factor of 10 will then rise ohmic power losses by a factor of 100.

As if that wasn't enough, forcing a certain current into a resistance-inductance-network (RL network) – what a series of cable, matrix and DUT represents – is taking linearly longer. That means 10 times the current takes 10 times the time:
E = P * t

The laws of physics and the DUT

What does that mean for the relays, cables and needles? When bringing these two physical laws together, you can estimate that raising the test current from 500 A to 1 000 A by a factor of 2 will raise the thermal energy within the relays, needles, and cables roughly by a factor of 8. Raising the current by a factor of 3 rises the thermal energy by a factor of 27, and raising the current by a factor of 10 raises the energy by a factor of 1 000.

Spreading this energy to more components – like using more parallel needles – is sometimes possible according to the design of the DUT. Especially on wafer-level and bare-die-level, there is no chance to raise the number of needles by these factors. This very often results in a compromise, which means lowering test currents to a level which could be handled.

Another challenge on wafer- and bare-die-level is that the silicon itself may not be stressed thermally since there is no proper possibility for cooling the DUT in that production stage.

The thermal power losses in a MOSFET are likely the same as in any other ohmic resistor, so the same rules may be applied as we did before for cabling, matrix, and so on. But there is one major difference: The amount of thermal energy which could be brought into the DUT is fixed and mainly defined by the thermal capacitance of the DUT. Assuming there is a working test setup for a testing current of 500 A and you wish to higher testing current to 1 000 A (which is assumed to be the DUT's specification), according to the above stated formula testing time has to be lowered at least by a factor of 4.

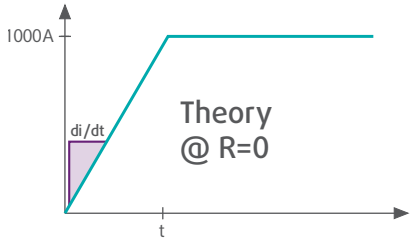

Figure 4 : Idealized current rise curve.

With a proper setup, 1000 A $R_{DS(on)}$ characterization nowadays can be performed below 300 µs. That is the point where the rise time of the current source and the inductance of cabling and matrix/multiplexer joins the game.

The initial current rise time in an RL-network is defined by the overall inductance of the whole setup and the applied voltage of the current source. With that stated, the source is forcing the current into the system with 50 V and the system has an overall inductance of 1 µH, the current rises with
di/dt = 50 V / 1 µH = 50 A*10^6/s= 50 000 000 A/s=50 000/ms=50 A/µs.
Therefore, the current of 1000 A would be settled within 20 µs (see figure 4). This would be the truth if not for the following facts:

- Current rise time of the source is limited
- Ohmic resistance is eating up the voltage

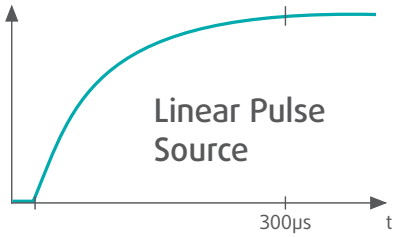

Figure 5 : Real current rise curve.

If the current rise time of your current source is the limiting fact, that could be solved easily. There are alternatives available on the market and the slow equipment can be replaced. The second problem needs a little bit more engineering and you need to take the total resistance of your test setup into account. Assuming a resistance of 40 m Ohm for cabling, matrix, needles, and DUT in total, there is a rising ohmic voltage drop with rising currents, which ends up by 40 V at 1000 A. This leads to the well-known curved e-function which is shown in the next figure. That e-function leads to a slower current settling (see figure 5). For a high speed 50 V current source, that would result in a pulse duration of X µs until the current is sufficiently settled.

Nowadays the following inductance and resistance could be archived by some simple tricks:

- Current pulse source 50 A/µs current slew rate
- Cabling <50 nH per meter, 1 mΩ per meter
- Matrix <250 nH, 10 mΩ
- DUT fixture: <100 nH, 1 mΩ
- DUT <5-50 nH, 1 mΩ

Figure 6: 1000 A pulse with one needle per contact.

With our demo test system at Electronica 2018, we realized $R_{DS(on)}$ test with 1000 A @ 300 µs by using only one power contact needle for source- and drain-pin of the DUT (see Figure 6).

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VX Instruments is one of nine Executive Members (total over 60 members) in the PXI System Alliance, the consortium, which defines and develops the PXI standard. Here we enjoy voting privileges and have direct access to the technical committee.

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The LXI Consortium is promoting the development and adoption of the LXI Standard, an open, accessible standard identifying specifications and solutions relating to the test and measurement industry.

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